REMARKS

Claims 1-9 and 12-19 were pending in the application. Claims 1-9, 12 and 14-15 have been amended. Claims 13 and 16-19 have been cancelled. Claims 20-22 are newly submitted. Accordingly, claims 1-9, 12, 14-15 and 20-22 remain pending in the application. No new matter has been added. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Double Patenting

Claims 1 and 16 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending U.S. Application No. 10/016,448.

A terminal disclaimer is enclosed to overcome the double patenting rejection.

II. The § 102 Rejections

Claims 1-9 and 12-19 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent. 6,829,751 to Shen et al. ("Shen").

Applicant respectfully traverses the rejections.

Claim 1, as amended, recites an application specific integrated circuit (ASIC) including a field programmable gate array (FPGA) coupled to a plurality of internal signals (including at least one bus) within the ASIC. The FPGA includes a debug client function that is in communication with a server and includes comparator logic operable to compare selected ones of the plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from the server, and includes storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

A. Shen Fails To Disclose an FPGA having a Debug Client Function That Includes Comparator Logic Operable To Compare Selected Ones of a Plurality of Internal Signals Coupled to the FPGA with a Trigger Pattern Downloaded from a Server

Shen discloses a system for designing an integrated circuit (IC) (see Abstract). More specifically, Shen discloses implementing an FPGA core that may be used to perform on-chip diagnostics that enable debugging functions, such as bus monitoring, probing, single step running, triggering, and capturing (col. 2, ll. 39-45). In operation, the FPGA core can be used to collect data from registers using a scan chain (col. 3, ll. 36-41). In particular, a user decides which signals need to be observed during a debugging period and, accordingly, the FPGA generates select signals that control which scan segments (of the scan chain) need to be accessed (col. 5, ll. 30-33; col. 4, ll. 35-58). After data is collected from the scan chains, the data is compressed and sent to a debugging workstation (col. 3, ll. 52-54). Shen further discloses that the system 100 of FIG. 1 (including the FPGA core and a debugging workstation) is operable to search for a specific signal pattern (col. 6, ll. 59-62).

While Shen may disclose collecting data within the FPGA core, Shen nevertheless fails to disclose the FPGA core includes comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server. In addition, while Shen discloses that the system 100 is operable to search for a specific signal pattern, Shen is silent as to specifically *how* the signal pattern is searched – i.e., it is not inherent that the FPGA core includes comparator logic for comparing selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern. *See* MPEP 2163.07 - "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or

possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Applicant respectfully submits that claim 1 is, therefore, allowable over Shen.

B. Other Independent Claims

Claim 9 incorporates limitations similar to those of claim 1.. Claim 9 (and the claims that depend therefrom) are also allowable over Shen for reasons corresponding to those set forth with respect to claim 1.

Independent claim 20 recites an ASIC including an FPGA connected to one or more of a plurality of software interfaces of the ASIC. The field programmable gate array (FPGA) includes a debug client function operable to manage instruction pointer logic associated with the one or more software interfaces connected to the FPGA.

Shen fails to disclose a field programmable gate array (FPGA) includes a debug client function that is operable to manage instruction pointer logic associated with the one or more software interfaces connected to an FPGA. Claim 20, and the claims that depend therefrom, are also allowable over Shen for at least this reason.

Applicant submits that claims 1-9, 12, 14-15 and 20-22 are allowable over the cited references, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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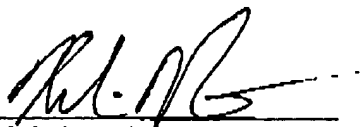

February 3, 2006
Date

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